IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: Pak *et al.*   Attorney Docket No.: SAND-P024B-CIP

Serial No.: Not yet assigned   Group Art Unit: 2819

Filed: Examiner: Le, D.

5 Title: Dynamic Circuit Using Exclusive States

PRELIMINARY AMENDMENT

The Commissioner of Patents and Trademarks

10 Washington, D.C. 20231

Sir:

IN THE SPECIFICATION

15

Please insert the following text underneath the title to claim the priority of the parent application:

--RELATED U. S. APPLICATION DATA--

On the next line, please insert --This Application is a Continuation-in-Part of U.S. Patent

20 application Serial No. 09/970,250, entitled "Dynamic Circuits Using Exclusive States" by Pak, et al., filed on 10/4/01.--

Please insert the following paragraph on page 6, line 12:

In one embodiment of the invention, the terms k, p, g can be defined as:

25   k (carry out termination/kill)   => -A & -B

     p (carry out propagation)   => A^ B or A+B

     g (carry out generation)   => A & B

where A and B are inputs such as A_0, B_0, A_1, B_1, A_2, B_2, A_3, B_3, as referenced in Figure

30 2.

Please insert the following paragraphs on page 6, line 20:

Additionally, the terms k, p, g can be defined in groups as follows:

5

$$gk \ (i{:}0) = k(i) + p(i) \ \& \ gk(i{-}1{:}0)$$
$$gp \ (i{:}0) = p(i) \ \& \ gp(i{-}1{:}0)$$
$$gg \ (i{:}0) = g(i) + p(i) \ \& \ gg(i{-}1{:}0)$$

10   For example, when $i = 1$, gk, gg, gp corresponds to $gk_{1\,0}$, $gg_{1\,0}$, $gp_{1:0}$, as referenced in Figure 2.

Also, for $i{>}j{>}k$,

15

$$gk(i{:}k) = gk(i{:}j) + gp(i{:}j) + gk(j{-}1{:}\ k)$$
$$gp(i{:}k) = gp(i{:}j) + gp(j{-}1{:}\ 0)$$
$$gg(i{:}k) = gg(i{:}j) + gp(i{:}j) + gg(j{-}1{:}\ k)$$

Group level inversions can be accomplished as a function of true terms as follows:

20

$$\sim gk(i{:}k) = gp(i{:}k) + gg(i{:}k)$$
$$\sim gp(i{:}k) = gg(i{:}k) + gk(i{:}k)$$
$$\sim gg(i{:}k) = gp(i{:}k) + gk(i{:}k)$$

25   In this embodiment, the terms k, p, g are mutually exclusive and the terms gk, gp, gg are mutually exclusive. By using exclusivity nature of the terms k/p/g and gk/gp/gg, inversion of signals can be expressed in terms of monotonic signals.

IN THE CLAIMS

Please add claims 30-42.

30.   (New) A dynamic adder to generate dynamic logic inversions, said dynamic adder comprising:

a dynamic circuit implementing a mutually exclusive circuit to indicate a three terms carry logic, wherein an inversion of any group of said three terms carry logic at the dynamic circuit is implemented as a function of true terms.

31.   (New) The dynamic adder of claim 30, wherein the three terms carry logic is propagate(p), generate (g), and kill (k)

32.   (New) The dynamic adder of claim 30, further comprising additional dynamic circuits arranged in levels to form a carry chain.

33.   (New) The dynamic adder of claim 30, wherein the groups of said three terms carry logic comprises group propagate (gp), group generate (gg), and group kill (gk).

34.   (New) The dynamic adder of claim 33, wherein the groups of said three terms carry logic are mutually exclusive.

35. (New) The dynamic adder of claim 34, wherein the inversion is implemented by $(\sim gk) = (gp) + (gg)$.

36.   (New) The dynamic adder of claim 34, wherein the inversion is implemented by $(\sim gp)=(gg)+(gk)$.

37.   (New) The dynamic adder of claim 34, wherein the inversion is implemented by $(\sim gg)=(gp) + (gk)$.

38.   (New) A method of implementing dynamic inversions in a carry chain
comprising the steps of:

implementing a three terms logic carry chain, wherein the three carry signals are
generate (g), propagate (p), and kill (k);

inversion of a group of said signals by utilizing a function, wherein said
function is a function of true terms.

39. (New) The method of claim 38, wherein the function is $(\sim gp)=(gg)+(gk)$.

40.   (New) The method of claim 38, wherein the function is $(\sim gg)=(gp)+(gk)$.

41.   (New) The method of claim 38, wherein the function is $(\sim gk)=(gg)+(gk)$.

42.   (New) The method of claim 38, wherein the groups of the three carry signals,
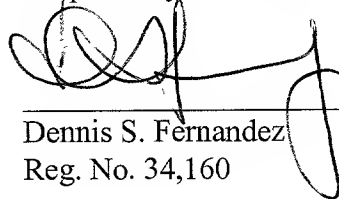(gg), (gp), and (gk) are mutually exclusive.

REMARKS

Newly added claims 30-42 relating to a dynamic adder are pending in this

5 application. Claims 4-29 are withdrawn from this Continuation-in-Part and stand pending

in the divisional application, Serial No. 09/970,250. Claims 30-42, supported by the

additional text added in the Specification, are submitted for further prosecution as a

Continuation-in-Part application of the parent application, Serial No. 09/970,250.

10 Attached hereto is a marked-up version of the changes made to the specification.

The attached page is captioned **"Version with markings to show changes made."**

In view of the above, it is respectfully submitted by Applicants that the claims are

in condition for allowance. Allowance of the claims at an early date is solicited.

15

Respectfully submitted,

20 Dennis S. Fernandez
Reg. No. 34,160

Date: 11/27/01

25 Address: Fernandez & Associates, LLP
PO Box D
Menlo Park, CA 94026-6204

Phone: (650) 325-4999
30 Fax: (650) 325-1203
Email: *iploft@iploft.com*

"VERSION WITH MARKINGS TO SHOW CHANGES MADE"

IN THE SPECIFICATION

Please insert the following text underneath the title to claim the priority of the parent application:

--RELATED U. S. APPLICATION DATA--

On the next line, please insert --This Application is a Continuation-in-Part of U.S. Patent application Serial No. 09/970,250, entitled "Dynamic Circuits Using Exclusive States" by Pak, et al., filed on 10/4/01.--

Please insert the following paragraph on page 6, line 12:

In one embodiment of the invention, the terms k, p, g can be defined as:

k (carry out termination/kill) $\Rightarrow$ -A & -B

p (carry out propagation) $\Rightarrow$ A^ B or A+B

g (carry out generation) $\Rightarrow$ A & B

where A and B are inputs such as A_0, B_0, A_1, B_1, A_2, B_2, A_3, B_3, as referenced in Figure 2.

Please insert the following paragraphs on page 6, line 20:

Additionally, the terms k, p, g can be defined in groups as follows:

gk (i:0) = k(i) + p(i) & gk(i-1:0)

gp (i:0) = p(i) & gp(i-1:0)

gg (i:0) = g(i) + p(i) & gg(i-1:0)

For example, when i = 1, gk, gg, gp corresponds to $gk_{1:0}$, $gg_{1:0}$, $gp_{1:0}$, as referenced in Figure 2.

Also, for i>j>k,

$$gk(i:k) = gk(i:j) + gp(i:j) + gk(j-1:k)$$
$$gp(i:k) = gp(i:j) + gp(j-1:0)$$
$$gg(i:k) = gg(i:j) + gp(i:j) + gg(j-1:k)$$

Group level inversions can be accomplished as a function of true terms as follows:

$$\sim gk(i:k) = gp(i:k) + gg(i:k)$$
$$\sim gp(i:k) = gg(i:k) + gk(i:k)$$
$$\sim gg(i:k) = gp(i:k) + gk(i:k)$$

In this embodiment, the terms k, p, g are mutually exclusive and the terms gk, gp, gg are mutually exclusive. By using exclusivity nature of the terms k/p/g and gk/gp/gg, inversion of signals can be expressed in terms of monotonic signals.

IN THE CLAIMS

Please add claims 30-42.

30.   (New) A dynamic adder to generate dynamic logic inversions, said dynamic adder comprising:

a dynamic circuit implementing a mutually exclusive circuit to indicate a three terms carry logic, wherein an inversion of any group of said three terms carry logic at the dynamic circuit is implemented as a function of true terms.

31.   (New) The dynamic adder of claim 30, wherein the three terms carry logic is propagate(p), generate (g), and kill (k)

32.   (New) The dynamic adder of claim 30, further comprising additional dynamic circuits arranged in levels to form a carry chain.

33.   (New) The dynamic adder of claim 30, wherein the groups of said three terms carry logic comprises group propagate (gp), group generate (gg), and group kill (gk).

34.   (New) The dynamic adder of claim 33, wherein the groups of said three terms carry logic are mutually exclusive.

35. (New) The dynamic adder of claim 34, wherein the inversion is implemented by $(\sim gk) = (gp) + (gg)$.

36.   (New) The dynamic adder of claim 34, wherein the inversion is implemented by $(\sim gp)=(gg)+(gk)$.

39.   (New) The dynamic adder of claim 34, wherein the inversion is implemented by $(\sim gg)=(gp) + (gk)$.

40.   (New) A method of implementing dynamic inversions in a carry chain comprising the steps of:

implementing a three terms logic carry chain, wherein the three carry signals are generate (g), propagate (p), and kill (k);

inversion of a group of said signals by utilizing a function, wherein said function is a function of true terms.

39. (New) The method of claim 38, wherein the function is $(\sim gp)=(gg)+(gk)$.

40.   (New) The method of claim 38, wherein the function is $(\sim gg)=(gp)+(gk)$.

41.   (New) The method of claim 38, wherein the function is $(\sim gk)=(gg)+(gk)$.

42.   (New) The method of claim 38, wherein the groups of the three carry signals, (gg), (gp), and (gk) are mutually exclusive.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Pak, et al.	
Application No.: 09/970,250	Art Unit No.: 2819
Filed: 10/4/01	
Title: Dynamic Circuit Using Exclusive States	Examiner: Le. D.
Attorney Docket No.: SAND-P024B-CIP	

Commissioner for Patents
Washington, D.C. 20231

CORRECTED DRAWING TRANSMITTAL LETTER

Sir:

Enclosed herewith please find:

( ) _____ sheets of redlined drawing(s) which indicate proposed changes to the drawing(s). Upon approval of these proposed changes, formal drawing(s) will be submitted.

( ) _____ sheets of substitute informal drawing(s) as required in 37 CFR 1.84(g). Please substitute the drawing(s) for the informal drawing(s) originally filed.

( ) _____ sheets of corrected formal drawing(s), as required by the Notice of Patent Drawings Objection (PTO-948) which accompanied the Office Action dated _____.

( ) _____ sheets of corrected formal drawing(s), as required by the Notice of Patent Drawing(s) Objection (PTO-948) and approved in the Notice of Allowability dated _____.

(X) _1_ sheet(s) of corrected drawing(s). Please substitute these corrected drawing(s) for the informal drawing(s) originally filed.

Examiner's approval of the entry of these drawings is respectfully requested. No new matter has been added.

I hereby certify that this correspondence is being deposited with the United States Postal Service as express mail in an envelope NO. ᛫᛫᛫ addressed to: Commissioner for Patents, Washington, D.C. 20231.

Date of Deposit. 11.29.01

Typed Name: Lora Paredes
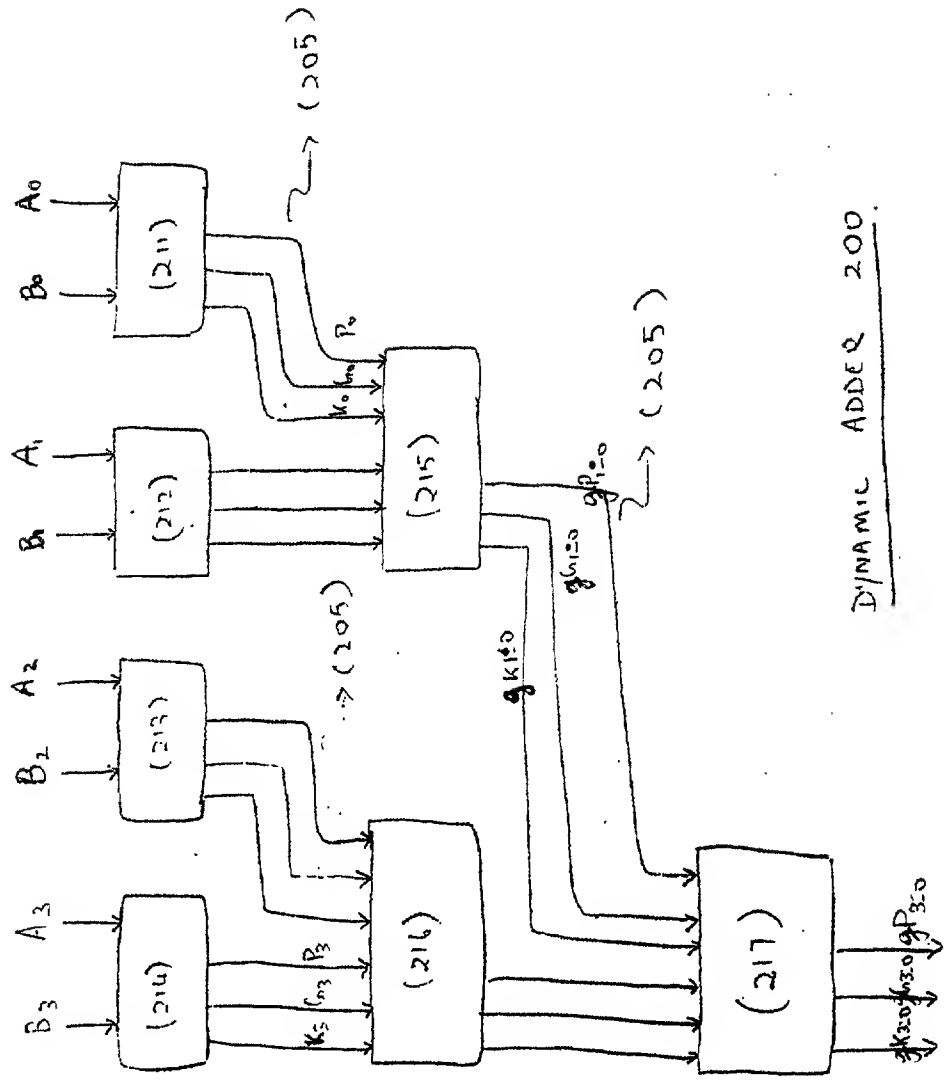
Signature: _____

Respectfully Submitted,

By _____
DENNIS S. FERNANDEZ, Esq
Reg. No. 34,160

Date: 11/27/01
Telephone:(650)325-4999

FIGURE - 2

DYNAMIC ADDER 200